 **ST.ANNE’S**

**COLLEGE OF ENGINEERING AND TECHNOLOGY**

(An ISO 9001:2015 Certified Institution)

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**QUESTION BANK**

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**SUB CODE/NAME:** EC8392 – DIGITAL ELECTRONICS

**EC8392-DIGITAL ELECTRONICS**

**UNIT-1**

## ****DIGITAL FUNDAMENTALS****

1. State the associative law of Boolean algebra.(May-8)[D]

2.State the distributive property of Boolean algebra (or) State distributive law.(Dec-13)[D]

3. Explain the De Morgan’s theorem in Boolean algebra.( May-11, 13)[D]

4. State two absorption properties of Boolean algebra.(Dec-4)[D]

5. Name the two canonical forms for Boolean algebra.(or) Name the two types of Boolean expressions.(May-7)[ID]

6.Express F=BC’+AC in a canonical SOP form.(Dec-3)[ID]

7. Simplify the following Boolean expression to a minimum number of literals.(Dec-5)[D]

 a) (X+Y) (X+Y’) b) XY+X’Z+YZ

8. Simplify the following Boolean expression.(May-5)[ID]

 ab’c’+ab’c +abc

9. Simplify: X+X’Y (Dec-7,May-10)[ID]

10.Show that expression[D]

 a) a+a’b=a+b b) x’y’z+x’yz+xy’=x’z+xy’

11. What is variable mapping? (May-7)[D]

12. What are don’t care conditions and incompletely specified function? (May-13)[D]

13.Show he karnaugh map with the encircled groups for the Boolean function, (May-6)[D]

 F=C’+A’D’+AB’D’

14. What are prime implicants?(Dec-5,8,13)[ID]

15.Write down the truth table of XOR gate. Give an application for XOR function.(May-8)[D]

16.Implement EX-OR gate using only NAND gate.(Dec-6)[D]

17. How can a NAND gate be used as an inverter? (May-4)[D]

19.Define noise margin.(May-5,7,8,Dec-3,4,8,10)[D]

22.Define tri-states.(Dec-3,10,May-5)[D]

24. Determine (377)10 in octal and Hexa-decimal equivalent. [D] **AU DEC 2014**

25. What is a karnaugh map?[D]

26. Define duality property.[D]

27. Simplify the Boolean expression ab’c+ab’c +abc.[ID]

28. Convert: [D]



29. Convert the given expression in canonical SOP form Y = AC + AB + BC[ID]

30. Show the k-map with the encircled groups for the Boolean function F= C’ +A’D’+AB’D’.[D]

**PART-B**

**FIRST HALF**

1. Prove the following Boolean identities. (May-7,8). Marks-8 [D]

 (x1+x2)(x’1x’3+x3)(x’2+x1x3)=x’1x2

1. Simplify he Boolean expression.(May-12) Marks-5 [D]

 F=x’y’z’+x’yz+xy’z’+xyz’

 3. Convert (A+B)(A+C)(B+C’) into standard POS form.(May-8) Marks-7[ID]

 4. Convert SOP to equivalent POS. (Dec-7) Marks-4[ID]

 A’B’C+A’B’C+A’BC+AB’C+ABC

 5. Express F=A+B’C as sum of minterms.(May-11,Dec-7) Marks-6 [ID]

 6. Express the Boolean function F=XY+X’Z in product of maxterm.(Dec-9) Marks-6 [D]

 7. Explain detail about number systems? [8] [D]

 8. Explain detail about various types Codes. [8] [D]

**SECOND HALF**

 9. Simplify the following expression using K-map method (Dec-13) Marks-10 [D]

 Y=∑m(7,9,10,11,12,13,14,15)

 10.Reduce the following function using Karnaugh map technique. (May-9) Marks-8 [D]

 F(A,B,C,D)= ∑m(5,6,7,12,13)+∑d(4,9,14,15)

 11. Express the following function as the minimal sum of products using a K-map.(May-5)

 Marks-12[D]

 F(a,b,c,d)=∑(0,2,4,5,6,8,10,15)+∑d(7,13,14)

 12. Simplify the following switching function using Karnaugh map.(Dec-3) Marks-12[D]

 F(A,B,C,D)=∑(0,5,7,8,9,10,11,14,15)+d(1,4,13)

 13.Simplify the given Boolean function into product of sum form using K-map.(May-13)

 Marks-8[D]

 F(A,B,C,D)=∑(0,1,2,5,8,9,10)

 14. Reduce the following function using K-map technique.(Dec-9) Marks-10[D]

 F(A,B,C,D)=π(0,3,4,7,8,10,12,14)+d(2,6)

 15. Simplify the following Boolean function by using a Quine McCluskey method.[D]

 F(A,B,C,D)=∑m(0,2,3,6,7,8,10,12,13) (Dec-9) Marks-16

 16. Obtain the minimum SOP using Quine McCluske’s mehod and verify using K-map.[ID]

 F=m0+m2+m4+m8+m9+m10+m11+m12+m13(Dec-6,10,Ma-7,9) Marks-8

 17. Determine the prime implicants of the following function and verify using K map.[ID]

 F(A,B,C,D)=∑(3,4,5,7,9,13,14,15) (May-9). Marks-16

 18. Simply using Quine McCluskey method and verify your result using K-map.[D]

 F=∑(0,1,2,5,7,8,9,10,13,15). (May-15) Marks-16

 19. Using Karnaugh map simplify the following expression and implement using basic

 gates.[D]

 F=∑(1,3,4,6) 2) F=∑(1,3,7,11,15)+d(0,2,5) (May-12) Marks-12

 20. Using K-map simplify the expression

 Y(A,B,C,D)=m1+m3+m5+m7+m8+m9+m0+m2+m10+m12+m13. Indicate the prime implicant sessential and non-essential prime implicants. Draw he logic circuit using AND-OR-INVERT gates and also using NAND gates. (May-6) Marks-16 [ID]

 21. Explain about NAND ands NOR implementations. (Dec-13)[D]

**UNIT-2**

### ****COMBINATIONAL CIRCUIT DESIGN****

 **TWO MARKS**

1.Enumerate some of the combinational circuits.(Nov/Dec-13)[D]

2. List out various application of Multiplexer. (Nov/Dec-13)[D]

3. Design Half subtractor using basic gates.(May/June-13)[D]

4. Draw the logic diagram of a 4 line to 1 line Multiplexer.(May/June-13) [D]

5. Draw the logic circuit of a 2 bit comparator.(May/June-14)[D]

6. What is priority encoder? (May/June-14)[D]

7. Draw the logic diagram of a serial adder.(Nov/Dec-12)[D]

8.Design a three bit even parity generator. .(Nov/Dec-12)[D]

9.Write the logic expression for the difference and borrow of a half subtractor.(April/May-11)[D]

10. Design a single bit magnitude comparator to compare two words A and B.(April/May11)[D]

11. construct 4- bit parallel adder/subtractor using full adder and XOR gates.(Nov/Dec-14)[D]

12. Convert a 2 to 4 line decoder with enable input to 1X 4 demultiplexer. (Nov/Dec-14)[D]

13. Draw the 2 bit comparator circuit using logic gates.(April/May-15).[D]

14.Write down the difference between demultiplexer and decoder.(April/May-15).[D]

15. Give the logic expression for sum and carry in full adder circuit.(April/May-15)[D]

16. Give examples for combinational circuits. .(April/May-15).[D]

17. What is code converter? List their types. (Vidyarthiplus.com)[D]

18. Suggest a solution to overcome the limitation on the speed of an adder. (Vidyarthiplus.com)[D]

19.What is difference between half adder and full adder?[D]

20. What is a data selector? Or What is multiplexer ? or Why is MUX called data detector?[D]

21. Mention the difference between DMUX and MUX.[D]

22. Give application of Demultiplexer.[D]

23. What is Demultiplexer?

24. What will be the maximum number of outputs for a decoder with a 6 bit data word?[ID]

25. Mention the uses of decoders. Or Application of decoder.[D]

26. What do you mean by encoder?[D]

27. Explain the design procedure for combinational circuits [D]

28. What is binary decoder?[D]

29. What do you mean by comparator[D]

1. Define Half adder and full adder[D]

**PART-B**

**FIRST HALF**

1. Design full adder using two half adders and an OR gate.(8) (April/May11) [D]

2. Design a 4 bit parallel adder/Subtractor and draw the logic diagram.(8) (Nov/Dec-

 12)11.[D]

3. Explain the working of carry-look ahead adder.(8) .(May/June-14) [ID]

4. How is carry look ahead adder faster than a ripple carry adder? Explain in detail with neat

 sketches.(8) (April/May-15).[ID]

5. Design BCD adder and explain its working with necessary circuit diagram. .(May/June-

 13) [D]

6. Draw the logic diagram of a BCD adder and explain its operation.(8) (Nov/Dec-12)[D]

7. Explain the operation of BCD adder.(8) (April/May11)[D]

8. Draw the logic diagram of BCD-Decimal decoder and explain its operation.[ID]

**SECOND HALF**

9. Draw the logic diagram of a 2-bit by 2-bit binary multiplexer and explain its operation.(8)

 (April/May11)[D]

10. Implement the following function using suitable multiplexer [D]

 F(A,B,C,D)=∑(1,3,4,11,12.13,14,15)(8) (April/May11)

11. Design 4\*1 Multiplexer circuit.(8) (April/May-15).[D]

12. Implement the function using Multiplexer F=∑(0,1,3,4,8,9,15).(8) (April/May-15).[D]

13. Design a full Subtractor using demultiplexers.(8) .(May/June-14)[D]

14. Design a 3:8 decoder using basic gates.(8) .(May/June-14)[D]

15. Draw the logic diagram of a 2-bit by 2-bit binary multiplexer and explain its operation.(8) (April/May11)[ID]

16. Implement the following function using suitable multiplexer [D]

 F(A,B,C,D)=∑(1,3,4,11,12.13,14,15)(8) (April/May11)

17.Design 4\*1 Multiplexer circuit.(8) (April/May-15).[ID]

18.Implement the function using Multiplexer F=∑(0,1,3,4,8,9,15).(8) (April/May-15).[D]

19. Design a binary to gray code convertor.(8) .(May/June-14)[D]

20. Design a four bit BCD to Excess-3 code convertor. Draw the logic diagram. (Nov/Dec12)[D]

21. Design a combinational circuit that converts 4 bit Gray code to a 4 bit binary number .Implement the circuit. (April/May-15).[D]

22. Draw the logic diagram of binary to octal decoder and explain the working in detail.(8) (April/May-15).[D]

22. Design & implement the conversion circuits for BCD to Excess – 3 code. (Vidyarthiplus.com)[D]

23. Design an Excess – 3 to BCD code converter. Uses don’t care . (Vidyarthiplus.com)[D]

24. Draw the block schematic of Magnitude comparator and explain its operations.(Nov/Dec13)

 [D]

25. Design 4 bit Magnitude comparator and draw the circuit. .(May/June-13)[D]

**UNIT-3**

#### ****SYNCHRONOUS SEQUENTIAL CIRCUITS****

**PART-A**

1. What is synchronous sequential circuit?(May-10,Dec-13)[D]

2. Define latch.(Dec-3)[D]

 3.Draw the circuit of SR flip-flop.[D]

4. Write reference to a JK flip-flop, What is racing?(May-4/Dec-8)[D]

 5. Differentiate between flip-flop and Latch.(may-5)[D]

6. What is drawback of SR F-F? How is this minimized?(May-6)[D]

 7.Draw the logic symbol and truth table of D F-F.(May-8)[D]

8. Differentiate between edge triggering and level triggering.(May-10)[D]

9.What is edge triggered flip-flop?(Dec-6,7)[D]

10. Realize JK flip-flop.(Dec-14)[D]

 11.Draw the logic circuit of a clocked JK flip-flop.(May-6)[D]

 12.Give the excitation table for JK flip-flop.(May-5,6,9,Dec-10)[D]

13.Obtain the excitation table of D and JK flip-flop.(May-5,9,Dec-10)[D]

14.Draw state diagram of SR flip-flop.(Dec-10)[D]

15.Convert JK FF to D FF.(May-3,5,7,Dec-3)[D]

16.Convert D flip-flop to T flip-flop(Dec-3,12,May-11,13).[D]

17.What is meant by programmable counter? Mention its application.(May-10)[D]

18.What is the minimum number of flip-flop needed to design a counter of modulus 60?[ID]

19. Define synchronous counter.(Dec-6)[D]

20.Draw the state diagram of MOD-10 counter.(Dec-8)[ID]

21.How many lip-flop are required to build a binary counter that counts from 0 to

 1023?(May-13)[D]

22.Write short notes on digital clock.(Dec-13)[D]

23. Define shift registers.(Dec-10)[D]

24. What are different types of shift type? Or Classify the registers with respect to serial and

 parallel input output?(Dec-10,May-7)[D]

25. If serial in serial out shift register has N stages and If the clock frequency is f, what will

 be time delay between input and output? (Dec-3)[D]

26. Draw a 2-bit ripple counter and convert this ino a 2-bit ring counter.(Dec-5)[D]

27. Design a 3 bit ring counter and find the mod of the designed counter.(Dec-12)[ID]

28. Give the comparison between synchronous and asynchronous sequential circuits.

 (Dec-10).[D]

29.Define state.[D]

 30.What is mealy machine? Give example(May-5,Dec-8) [D]

31.Compare Moore and Mealy model(May-9,Dec-10)[D]

32.Explain about state reduction or Why is state reduction necessary?(Dec-4,6,May-9)[D]

**PART-B**

**FIRST HALF**

1.Explain the working of a master-slave JK flip-flop?(May-03,05,08,Dec-03,06,08,09)

**Or**

 Describe the input and output action of JK master/slave flip-flop.(May-5) Marks-8[D]

1. Realize a SR flip-flop using NAND gates and explain its operation.(Dec-3) Marks-10 [D]
2. Draw the logic diagram of a D-FF using NAND gates and explain.(Dec-8) Marks-6[D]
3. Draw the block diagram of SR –FF and explain.(Dec-13) Marks-6[D]
4. How will convert a D flip-flop into JK flip-flop.(Dec-9) Marks-8[D]
5. Convert D flip-flop into T flip-flop (May-11, Dec-12) Marks-6 [D]
6. Draw RS flipflop circuit and explain its operation with truth table and suggest how to

 eliminate the undetermined stage? Write RS flipflop applications.[dec-17] [ID]

 Mark-13

**SECOND HALF**

1. Explain in detail the operation of a 4-bit binary ripple counter. (Dec-9) Marks-16 [D]
2. Design and explain the working of an up-down ripple counter.(May-3) Marks-8[D]
3. Explain the design steps of Mod n counter.(May-12) Marks-8 [ID]
4. Design a 3-bit synchronous counter using JK flip-flop.(Dec-14) Marks-12[D]
5. Draw a 4-bit serial-in-serial-out shift register and draw its waveforms. (May-6, Dec-6)

 Marks-8 [D]

1. Draw a 4-bit parallel-in-serial-out shift register and briefly explain.(May-6) Marks-8

 [D]

1. Explain the operation of universal shift register with neat block diagram.

 (Dec-8,10,May-9)marks10[D]

1. Draw the 4-bit Johnson counter and explain the operation.(May-7,Dec-6) Marks-

 8.[ID]

1. Explain the operation of shift and Ring counters.(May-12) Marks-8 [D]
2. Design a 4 bit bi-directional shift register.(Dec-12) [D]
3. Explain the steps involved in the reduction of state table.(Dec-10) Marks-10 [D]

18. Design a 4 bit binary counter and explain its counting process. Discuss how to use this

 circuit to perform both up and down counting. .[dec-17] [D] Mark-13

19. Design and explain the working of a synchronous mod-3 counter.[May-17] [ID] mark-13

**UNIT-4**

**ASYNCHRONOUS SEQUENTIAL CIRCUITS**

**PART-A**

1. What are hazards?(May-9, Dec-9,13,May-13) [D]
2. What are the two types of hazards?[D]
3. Define static hazard. How it can be avoided?(May-9)[D]
4. What are the hazard free digital circuits? (may-10)[D]
5. Explain dynamic hazard. (Dec-8)[D]
6. What is an asynchronous sequential circuit? (Dec-4)[D]
7. What is fundamental mode asynchronous sequential circuit? (May-, Dec-3)[D]
8. Define flow table in asynchronous sequential circuit.( May-7,Dec-6,7).[D]
9. Define primitive flow table. (Dec-8)] [D]

10.What is cycle? Or When does a cycle occur?(May-3,5)[D]

 11.What are races? (May7, Dec6,7,8)[D]

 12. Define critical race? (May-6Dec7,10)[D]

 13. What is the cause of essential hazard? (May ,Dec4).[D]

 14.What are static-0 and staic-1 hazards?[D]

 15. How does the operation of an asynchronous input differ from that of a syncconous

 input? (Dec5) [ID]

 16. What are the types of asynchronous circuits?[D]

 17.Define noncritical race.[D

 18. What is synchronous sequential circuits?[D]

 19. What are the types of asynchronous circuits? [D]

 20. What is pulse mode circuit?

 21. What are the significance of state assignment?

 22. What are the different techniques used in state assignment [May-16] [D]

 23. How can a race be avoided? [D]

 24. what is the cause of essential hazard?[May-3] [ID]

 25. Write short note on one hot state assignment.[D]

 26. What is fundamental mode.[D]

 27. Define total state[D]

 28 . What is static 1 hazard?[D]

 29. What is static 0 hazard?[D]

 30.Give the comparison between synchronous & Asynchronous counters.[D]

**PART-B**

**FIRST HALF**

1. What are called as essential hazards? How does the hazard occur in sequential

 circuits? How can the same be eliminated using SR latches? ( may-10). Marks-16[D]

1. List and explain the steps used for analyzing an asynchronous sequential circuit.

 (dec-10, May-11) Marks-8.[D]

1. When do you get the critical and noncritical races? How will you obtain race free

 condition? (Dec-10)Marks-10[D]

1. Write a short note on hazard free switching circuits.(May-12) Marks-8[D]
2. What is hazard? Explain the different types of hazard. What is an essential hazard?(Dec-12) Marks-16[D]
3. What is a hazard in an asynchronous sequential circuits? Define static hazard,

 dynamic hazard and essential hazard. (dec-14) Marks-8[D]

1. Design a hazard-free asynchronous circuit that changes state whenever the input

 goes from logic 1 to logic 0. (May-1). Marks-16[D]

1. Illustrate mixed operating mode sequential circuit model.(dec-6, May-7) Marks-8[ID]
2. Race condition in asynchronous sequential circuits. (Dec-11,12) Marks-8[D]
3. Write explanatory notes on algorithmic state machine. OR Illustrate the design procedure of algorithmic state machine with neat flow chart. (May/June-13) Marks-8[ID]

 8[D]

 11. Briefly explain the dynamic and essential hazards. Marks-8 [Dec-8] [D]

**SECOND HALF**

 12. What is objective of state assignment in a asynchronous circuit? Give the hazard free

 realization for the Boolean function f(A,B,C,D)=Σm(0,2,6,7,8,10,12) May-17 Marks-13

 [D]

 13. Design an asynchronous sequential circuit with two inputs X1 andX2 and with one

 output Z. When X1 is 0 the output Z is o. The first change in X2 that occurs while X1 is

 1will cause output Z will remain 1 until X1 returns to 0. May-16 [D] marks-13

 14. Design a asynchronous sequential circuit with 2 inputs T and C. The output attains a

 value of1 when T=1 and C moves from 1 to 0. Otherwise the output is 0. Dec-15 [D]

 Marks-13

15. Explain the different methods of racefree state assignment.Dec-15 [D] Marks-13

16.Derive the ASM chart for binary multiplier. May-15 Marks -8 [D]

17. Explain the ASM chart. Marks -8 [D]

**UNIT-5**

**MEMORY DEVICES AND DIGITAL INTEGRATED CIRCUITS**

**PART-A**

1. How many location are addressed using 18 address bits?(Dec-8)[D]

2. Define a memory location and a cell.(May-6)[D]

 3. Which memory is called volatile? Why?.(Dec-13,7)[ID]

 4. Name the types of ROM.(May-11).[D]

5. What is non-volatile memory(Dec-13)[D]

 6. What is meant by static and dynamic memories?(May-6)[D]

7. How is individual location in a EEPROM programmed or erased?(May-6)[D]

8. Mention the two types of erasable PROM.(Dec-6)[D]

9. Whether ROM is classified as non-volatile storage device?Why?(Ma-7)[D]

10. What is RAM? (Dec-6)[D]

11. Give the advantage of RAM.(Dec-13)[D]

12. Compare and contrast static RAM and dynamic RAM. (Or) What are the advantage of

 static RAM compared to dynamic RAM?(Dec-9,May-10)[D]

13. Draw the basic dynamic memory cell. (Or) Draw the logic diagram dynamic RAM

 cell.(Dec-6) [D]

 14. What is write cycle time? P(or) What is write memory cycle? (May-8)[ID]

15. What is meant by memory expansion? Mention its limit.(May-10)[D]

16. Give he classification of PLDs.(May-13)[D]

17. What is a PLA?(May-8)[D]

18. Compare the features of PROM, PAL and PLA?(or) Distinguish between PLA and

 PAL?(May-9) [D]

19. What is a combinational PLD?(Dec-7)[D]

20. What is FPGA?(DEC-4,14,May-6)[D]

21. Define address and word:[D]

22. State the types of ROM [D]

23. Explain EEPROM. [D]

24.Explain PROM. [D]

25. Define PLD. [D]

26.What is the memory capacity of random access memory if it has 10 bit address lines?

 [Dec-7] [D]

27.Differentiate between PAL and PLA.[Dec7][D]

28. How the bipolar RAM Cell is different from MOSFET RAM cell?[May-16][D]

29.What is read and Write operation?[Dec-15][D]

30. What is the basic difference between the RAM and ROM circuity?[May-15][D]

31.State advantage and disadvantage of CMOS.(Dec-3)[D]

 32.Classify the basic families that belong to the bipolar families and to the MOS families.

 (May-6)[D]

**PART-B**

**FIRST HALF**

1.Compare static RAMs and dynamic RAMs.(Dec-9, May-12). Marks-8.[D]

2. Explain the principle of operation of bipolar SRAM cell.(May-10).Marks-8[D]

3. Explain read and write operation of memory with timing waveforms.(dec-10). Marks-8[ID]

4. Discuss the classification of ROM and RAM memories.(May-12).Marks-8[D]

5. Describe the concept ,working and application of FPGA. (Dec-10,May-12,dec-13).Marks-8[D]

6. Given the classification of semiconductor memories. (Dec-12,17). Marks-16[ID]

7. Explain the memory decoding.(May-12,Dec-12). Marks-8[D]

8. Briefly explain the EPROM and EEPROM technology.(May-11).Marks-6[D]

9. With logic diagram, explain the basic macrocell. (May-11) .Marks-8.[D]

10. Discuss the features and functional blocks of FPGA[Dec17] Marks-13[D]

11. Write short notes on : i) PAL ii) FPGA [Dec-16] marks 13[D]

12. Implement the following function using PLA. [May-16] marks-13[D]

 F1(x,y,z)=Σ(1,2,4,6) F2(x,y,z)=Σm(0,1,6,7) F3(x,y,z)=Σm(2,6)

13. Compare the RAM,ROM,PROM and EPROM [May-15] marks-8[D]

14. Use PLA with 3 inputs ,4 AND terms and two outputs toimplement thefollowing two Boolean

 Functions[ID]

 F1(A,B,C)=Σm(3,5,6,7) and F2(A,B,C)=Σm(1,2,3,4)

15. Design ROM forvthe following functions f1=Σ(1,2,3); F2=Σ(0,2) May-11 marks 07[D]

16. Design a combinational circuit using ROM . The circuit accepts 3-bit number and generate an output binary number equal to square of input numbers. [May-10,11] [ marks-13][ID]

17. Draw a PLA circuit to implement the logic functions. [Dec-7] Marks- 6[D]

 A’BC+ AB’C+AC’ and A’B’C’+BC

18.Implement the following two Boolean functions with a PLA. Marks- 8[D]

 F1(A,B,C) =Σm(0,1,2,4) F2(A,B,C) =Σm(0,5,6,7)

19. Tabulate the PAL programmable table for the four Boolean fubnctions listed below.(May-16)

 marks-8[D]

 A(x,y,z) =Σm(1,2,4,6) B(x,y,z) =Σm(0,1,6,7) C(x,y,z) =Σm(2,6)

 D(x,y,z) =Σm(1,2,3,5,7)

**SECOND HALF**

20.Explain the concept, operation and characteristics of TTL family.(Dec-10) Maks-8[D]

21.Draw the TTL inverter ciruit.(Dec-4,May-12) Marks-10[D]

22..Explain the concept, operation and characteristics CMOS family.(Dec-10) Marks- 8 [D]